Hall Ticket No.: | | | | | | | | | | |

Set-1

Course Code: **23MTVLT01**

MALINENI LAKSHMAIAH WOMEN'S ENGINEERING COLLEGE

(AUTONOMOUS)

I - M.Tech. I - Semester (MR23) Regular Examinations, March - 2024

CMOS DIGITAL IC DESIGN

Department of Electronics & Communication Engineering

Time: 3 hours Max. Marks: 75

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*Answer **ALL** the questions – **5*15=75 Marks***

Q. No.		Question	Marks	CO	BL
1	a)	Define Threshold Voltage. Express threshold voltage and discussdependency of VT on various parameters.	(7M)	CO1	L3
	b)	Explain the voltage transfer characteristics of a CMOS inverter with a neat diagram.	(8M)	CO1	L4
		(OR)			
2	a)	Discuss about body effect and threshold of a MOS device.	(10M)	CO1	L4
	b)	Determine the pull-up to pull-down ratio for an NMOS inverter.	(5M)	CO1	L4
3	a	Design and implement AOI and OIA using CMOS.	(10M)	CO2	L3
	b	Write short notes on transmission gates with the relevant circuits.	(5M)	CO2	L4
		(OR)			
4	a	Realize full adder using CMOS discuss.	(10M)	CO2	L3
	b	Design and explain the operation of 2 input NMOS NAND.	(5M)	CO2	L3
5	a	Realize CMOS D flip flop and discuss.	(10M)	CO3	L4
	b	Write short notes on SR latch in sequential MOS logic.	(5M)	CO3	L4
		(OR)			
6	a	Draw the logic diagram of a CMOS clocked SR flip-flopandexplain with the help of a truth Table.	(8M)	CO3	L4
	b	Differentiate static and dynamic latches.	(7M)	CO3	L3
7	a	Explain the speed and power dissipation in dynamic CMOS logic.	(7M)	CO4	L3
	b	What are the various issues in CMOS dynamic logic design? Explain anyone with a neat sketch.	(8M)	CO4	L3
		(OR)			
8	a	Write short notes on Dynamic pass transistor.	(6M)	CO4	L3
	b	Explain voltage boots trapping with an example.	(9M)	CO4	L3
9	a	Mention different types of RAM cells. Draw and explain the operation of a single bit dynamic RAM	(15M)	CO5	L4
		(OR)			
10	a	Explain NOR flash memory.	(7M)	CO5	L3
	b	Write about the leakage currents in SRAM.	(8M)	CO5	L3

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